9.7 A 7ps-Jitter 0.053mm² Fast-Lock ADDLL with Wide-Range and High-Resolution All-Digital DCC

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As the operating frequencies of high performance SoCs and memories increase beyond 1 GHz, the quality of the DLL used to synchronize the clock and data becomes critical. Thus low power, small jitter, fast lock time and 50% duty cycle become important goals in DLL design. The conventional clock-synchronized delay (CSD) scheme is an all-digital open-loop type that achieves fast lock time but suffers from bad resolution and narrow operating range at a low-voltage [1]. The conventional open-loop duty cycle corrector (DCC) achieves fast lock time and 50% duty cycle ratio of the output clock [2]. However, as the operation frequency increases, it requires large area and power due to additional delay lines with control blocks to achieve high resolution and wide frequency range. This paper describes an all-digital DLL (ADDLL) that achieves low jitter, fast lock time and 50% duty cycle correction with an open-loop scheme. It operates over a wide frequency range, from 440MHz to 1.5GHz, with maximum lock-in time of 15 cycles. The peak-to-peak jitter is 7ps at 1.5GHz and the power consumption is 43mW at a 1.8V supply.

Figure 9.7.1 shows the block diagram of the proposed ADDLL and all-digital DCC (ADDCC). The open-loop ADDLL comprises a main delay line (MDL), a coarse code generator (CCG), a fine code generator (FCG) to control the signal precisely, a range doubler and other control blocks for signal selections and phase error reduction. The conventional CSD type achieves a fast lock time but has a critical problem of poor resolution at high frequencies. The proposed DLL has a similar configuration to the CSD but has solved the resolution problem by adopting the FCG. The open-loop ADDCC consists of a cycle detector for detection of one-cycle delayed clock of an input and generation of its half-cycle delayed clock, a weighted signal generator (WSG) for adjusting phase errors of the falling edge, an edge generator for generating an output of 50% duty cycle ratio and a falling-edge control block. The conventional digital DCC suffers from a trade-off between resolution and operation range as the operating frequency increases. The proposed ADDCC has overcome this problem with the WSG and the dual delay line in the cycle detector.

Figure 9.7.2 is the timing diagram of the ADDLL, where the upper diagram illustrates the overall operation of the system including ADDCC and the lower diagram illustrates that of the ADDCC. The basic operation of ADDLL follows that of the CSD type. The CCG generates cds<i> signals that are synchronized with In_clk. The MDL selects the same signal path of mds<i> as the cds<i> because an identical delay line is used in the CCG and the MDL. After the FCG precisely tunes mds<i> and the phase mixer mixes amds<i> with mds<i>, the output clock becomes synchronized with the Ref_Clk after the duty cycle correction process. The low-power CCG with a limited number of delay cells detects only a narrow range of input signals. Thus, the range doubler delays the input signal by T_{delay} to double the detection range with negligible increases of power and area when the input clock (In_clk) period becomes longer than the first detectable range. The operation principle of the ADDCC is as follows. DLL_Out signal enters the ADDCC and the cycle detector generates a one-cycle delayed clock (CS<i>) and a half-cycle delayed clock (HS<i>) of the DLL_Out. The ADDCC adjusts the duty-cycle ratio of DLL_Out to 50% as the rising edge of the final output of ADDCC, Clkout, is generated at the rising edge of DLL_Out and the falling edge of the Clkout is generated at the rising edge of Hclk. However, Hclk may have a phase error such that ADDCC cannot generate an exact 50% duty-ratio clock. To solve this problem the phase error is detected and reduced by the proposed WSG. The falling-edge control block detects the magnitude of the phase error and generates control signals (DL_SW, CE). Then, the WSG compensates the phase error as it delays the Hclk by 0.75τ, 0.875τ, 1.125τ and 1.25τ according to the control signals while DLL_Out is delayed by 1τ.

To increase the resolution of the ADDLL, we propose the FCG, shown in Fig. 9.7.3. It consists of a fine code detector (FCD), a self-calibration circuit (SCC) and a tuned delay line. The FCD generates a select signal (cont) and 4b codes (F<1:4>) for fine tuning the ADDLL. It compares the phase of cds<n> with the phase of In_Clk. If one leads the other, the tuned delay line delays its phase according to the tuning factor *K*. This operation continues until the cont signal and 4b codes are generated. Each tuned delay line has two buffers. One is fixed and the other is tunable which is realized by adjusting the size of transistors. The *K* factor is dependent on the unit delay (τ) of the MDL. Therefore, it determines the finest delay resolution to reduce errors. In the conventional asynchronous binary search type, the phase detector (PD) has jitter components due to PVT variations [3]. To reduce jitter generated by the PD, the SCC is implemented. It consists of a delay line similar to that of the MDL, using a phase interpolator and the identical PD to those of the FCD. It measures setup time variations of the PD due to PVT variations. Its output signals (Sf<n>) adjust the delay factor *J* of the extra delay, which adjusts the delay of In_Clk while cds<n> is delayed by an amount of dummy delay (1τ). As a result, the PD in the FCD operates insensitively to PVT variations.

Figure 9.7.4 is the block diagram of the cycle detector used in the ADDCC. It consists of an upper delay line with a unit delay of 1τ and a lower delay line with a unit delay of 2τ. Conventional DCCs and DLLs use a single delay line to detect a synchronized position whose operation range is limited [2,4]. To achieve a wide operating frequency range, a dual delay line is used which does not require complex hardware overhead to make more select signals, S_{sel}. Therefore, the ADDCC, with an area increase of only 7%, doubles the operating frequency range without consuming additional power by using DL_SW signal to select and use only one delay line at a time. The cycle detector detects the synchronized clock for two cycles, which is a margin until switching to another delay line. If all S_{sel} are low, which means it cannot find the synchronized clock with the first delay line within two cycles, the second delay line is selected to find it. When an S_i is high, it outputs a CS<j> to measure a phase error and an HS<j> to generate the falling edge of the output clock.

The measured results of the proposed ADDLL are shown in Fig. 9.7.5. The waveforms on the left show an output clock with a duty cycle ratio of 50.6% corrected from a 69.9% duty-cycle ratio input clock with a phase error of 17.1ps between the input and the output clock. The measurement result with a quiet supply shows jitters of $7ps_{pp}$ and $0.9367ps_{rms}$ at 1.5GHz, as shown on the right of Fig. 9.7.5. Figure 9.7.6 summarizes the performance comparison of the proposed ADDLL with conventional high-speed types. Figure 9.7.7 is the chip micrograph of the core circuit, which occupies an area of $0.053mm^2$.

Acknowledgement:
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References:

[1] T. Saeki, K. Minami, H. Yoshida, and H. Suzuki, "A Direct-Skew-Detect Synchronous Mirror Delay for Application-Specific Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 372-379, Mar., 1999.

[2] C. Jeong, C. Yoo, J.J. Lee, and J. Kih, "Digital Delay Locked Loop with Open-loop Digital Duty Cycle Corrector for 1.2Gb/s/pin Double Data Rate SDRAM," *ESSCIRC*, pp. 379-382, 2004.

[3] J. Wang, Y. Wang, C. Chen, and Y. Liu, "An Ultra-Low-Power Fast-Lock-In Small-Jitter All-Digital DLL," *ISSCC Dig. Tech. Papers*, pp. 422-423, Feb., 2005.

[4] B.W. Garlepp, K.S. Donnely, J. Kim, et al., "A Portable Digital DLL for High-Speed CMOS Interface Circuits," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 632-643, May, 1999.

[5] J.-T. Kwak, C.-K. Kwon, K.-W. Kim, et al., "A Low Cost High Performance Register-Controlled Digital DLL for 1Gbps x32 DDR SDRAM," *Symp. VLSI Circuits*, pp. 283-284, Jun., 2003.

[6] Y.J. Jeon, J.-H. Lee, H.-C. Lee, et al., "A 66-333MHz 12-mW Register-Controlled DLL with A Single Delay Line and Adaptive-Duty-Cycle Clock Dividers for Production DDR SDRAMs," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2087-2092, Nov., 2004.

[7] H.-H. Chang and S.-I. Liu, "A Wide-Range and Fast-Locking All-Digital Cycle-Controlled Delay-Locked Loop," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 661-670, Mar., 2005.

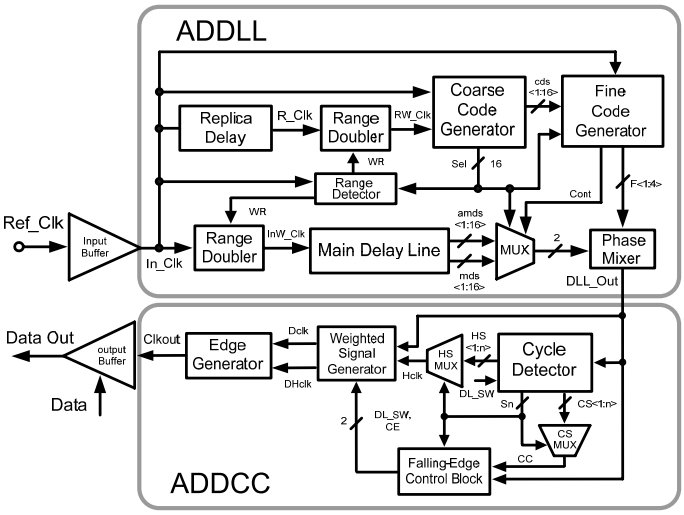

Figure 9.7.1: Block diagram of the proposed ADDLL and ADDCC.

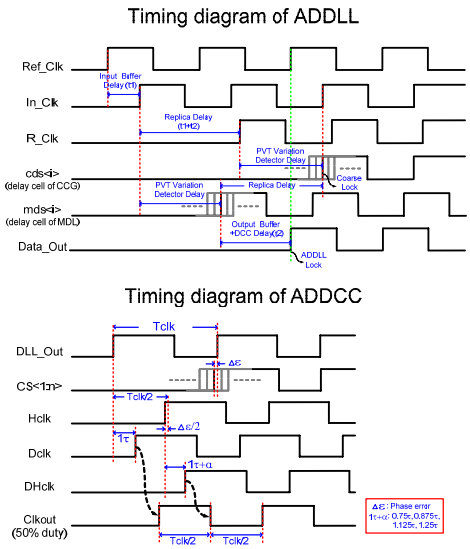

Figure 9.7.2: Timing diagrams of ADDLL and ADDCC.

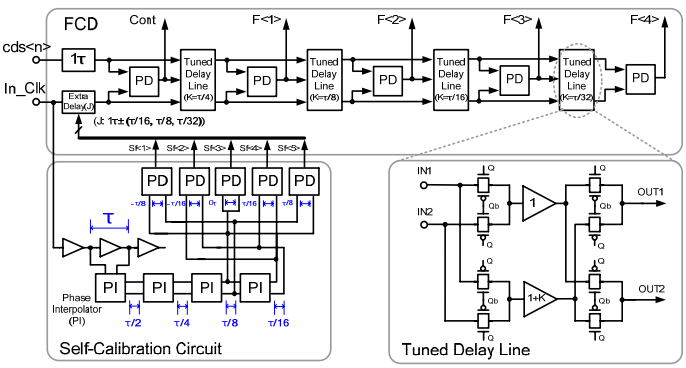

Figure 9.7.3: Fine code generator with self-calibration circuit.

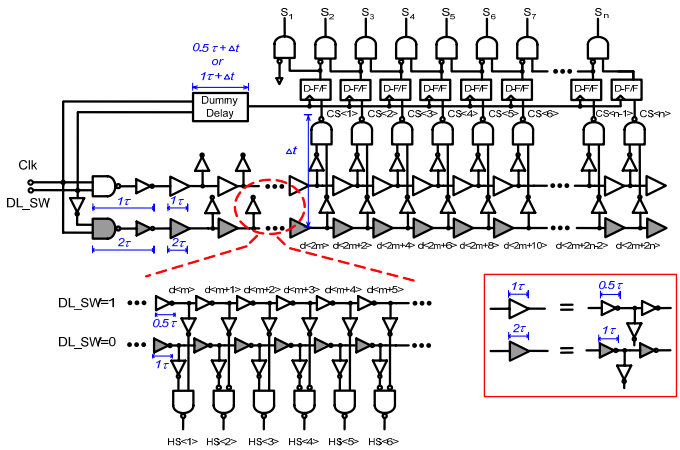

Figure 9.7.4: Cycle detector using dual delay lines for wide frequency range.

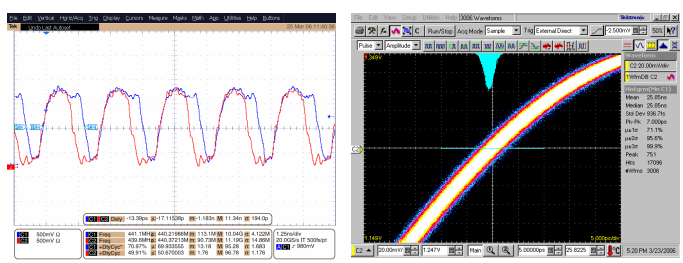

Figure 9.7.5: The measured waveform and jitter histogram.

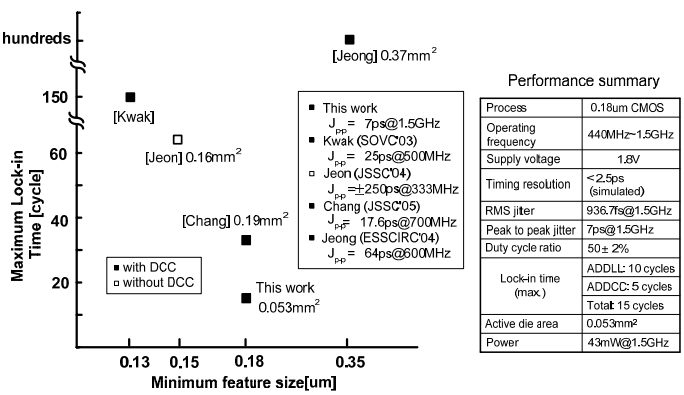

Figure 9.7.6: Performance summary and comparison.

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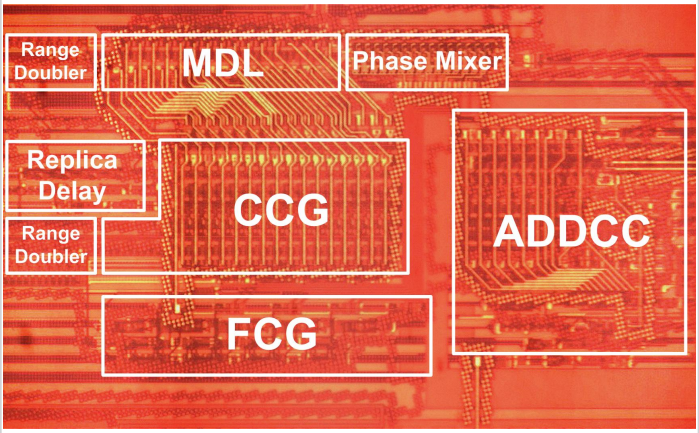

Figure 9.7.7: Chip micrograph.

